

CLAIMS

We Claim:

- 1 1. An apparatus comprising:
 - 2 a controller to generate command signals to a device to access the device to
 - 3 transfer data between the device and a bus coupled to the device; and
 - 4 a flag signal generation unit to generate a flag signal to the device to trigger the
 - 5 data transfer between the device and the bus in response to a state transition that occurs in
 - 6 the flag signal after a specified period following a data transfer command, but said flag
 - 7 signal to also initiate a different command than the data transfer command in response to a
 - 8 state transition that occurs in the flag signal within the specified clock period.
- 1 2. The apparatus of claim 1 wherein the data transfer command is a read or write
- 2 command and the different command is a precharge command.
- 1 3. The apparatus of claim 2 wherein the device is a memory device.
- 1 4. The apparatus of claim 1 wherein the memory device is a dynamic-random-access-
 - 2 memory, DRAM, which responds to a read or a write command to perform a
 - 3 corresponding data transfer between the DRAM and the bus if the flag signal has a
 - 4 transition after the lapse of a specified clock period, but first performs an auto-precharge
 - 5 on at least one bit line of the DRAM selected for the read or the write command if the flag
 - 6 signal has a transition within the specified clock period following the read or the write
 - 7 command.
- 1 5. The apparatus of claim 4 wherein the specified clock period is one clock period
- 2 following the data transfer command.

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1 6. An apparatus comprising:
 2 a memory array to couple to a data bus to transfer data between said memory array
 3 and bus in response to a command signal received to initiate the data transfer; and
 4 a timing unit coupled to receive the command signal to initiate the data transfer
 5 and also coupled to receive a flag signal to trigger the data transfer, said timing unit to
 6 interpret the flag signal to determine if the flag signal has a transition prior to a lapse of a
 7 specified clock period following the command signal and to perform a different command
 8 operation than data transfer, if the flag signal has a transition prior to the lapse of the
 9 specified clock period following the command signal.

1 7. The apparatus of claim 6 wherein the command signal is to perform a read or write
 2 operation and the different command operation is a precharge operation.

1 8. The apparatus of claim 6 wherein said timing unit generates an internal flag signal
 2 to trigger the data transfer if a transition of the flag signal occurs after the specified clock
 3 period following the command signal, but to generate an auto-precharge signal if a
 4 transition of the flag signal occurs prior to the lapse of the specified clock period following
 5 the command signal.

1 9. The apparatus of claim 8 wherein the command signal is to perform a read or write
 2 operation and the different command operation is an auto-precharge operation.

1 10. The apparatus of claim 9 further including a decoder coupled to the memory array
 2 to decode the command signal and at least one control circuit to perform the data transfer
 3 between said memory array and the data bus.

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1 11. The apparatus of claim 10 wherein the apparatus is a dynamic-random-access-
2 memory, DRAM.

1 12. The apparatus of claim 10 wherein the specified clock period is one clock period
2 following the data transfer command.

1 13. A system comprising:

2 a controller to generate a data transfer command signal to effect data transfer and
3 also to generate a flag signal to time triggering of the data transfer;

4 a memory device coupled to said controller to receive the data transfer command
5 signal and transfer data in response to the data transfer command signal;

6 a bus coupled to said memory device to transfer data between said memory and
7 bus in response to the data transfer command signal;

8 said controller to generate the flag signal to the memory device to trigger the data
9 transfer between the memory device and the bus in response to a state transition that
10 occurs in the flag signal after a specified clock period following the data transfer
11 command signal, but said flag signal to also initiate a different command signal than the
12 data transfer command signal in response to a state transition that occurs in the flag signal
13 within the specified clock period; and

14 said memory to receive and interpret the flag signal to determine if the flag signal
15 has a transition within the specified clock period following the command signal and to
16 perform a different command operation from data transfer, in response to a transition
17 present in the specified clock period following the data transfer command signal.

1 14. The system of claim 13 wherein said memory device is a dynamic-random-access-
2 memory, DRAM.

1 15. The system of claim 14 wherein the different command signal is a precharge
2 command.

1 16. The system of claim 13 wherein the data transfer command is a read or write
2 command and the different command is an auto-precharge command associated with the
3 read or write command.

1 17. The system of claim 16 wherein said controller is a memory controller.

1 18. The system of claim 16 further comprising a processor, wherein said controller is a
2 memory controller coupled to said processor.

1 19. A method comprising:
2 issuing a command signal;
3 generating a flag signal in response to the issuing of the command signal to trigger
4 a response to a corresponding operation of the command signal after a lapse of a specified
5 time period following the issuing of the command signal; and
6 coding a different command on the flag signal by having the flag signal transition
7 within the specified time period following the issuing of the command signal to perform a
8 different operation than the corresponding operation of the command signal.

1 20. The method of claim 19 further comprising receiving the command and flag
2 signals and interpreting the flag signal to determine if a transition is present within the
3 specified time period following the issuing of the command signal.

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1 21. The method of claim 20 wherein the different operation of the different command
2 signal is a precharge operation of a memory.

1 22. The method of claim 20 wherein the command signal issues a read or write
2 command to memory to perform a read or write operation.

1 23. The method of claim 22 wherein the different operation of the different command
2 signal is an auto-precharge operation, which is performed prior to performing the read or
3 write operation.

1 24. The method of claim 23 wherein the command and flag signals, including the
2 coding of the different command signal in the flag signal, are issued to a dynamic-random-
3 access-memory, DRAM.

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